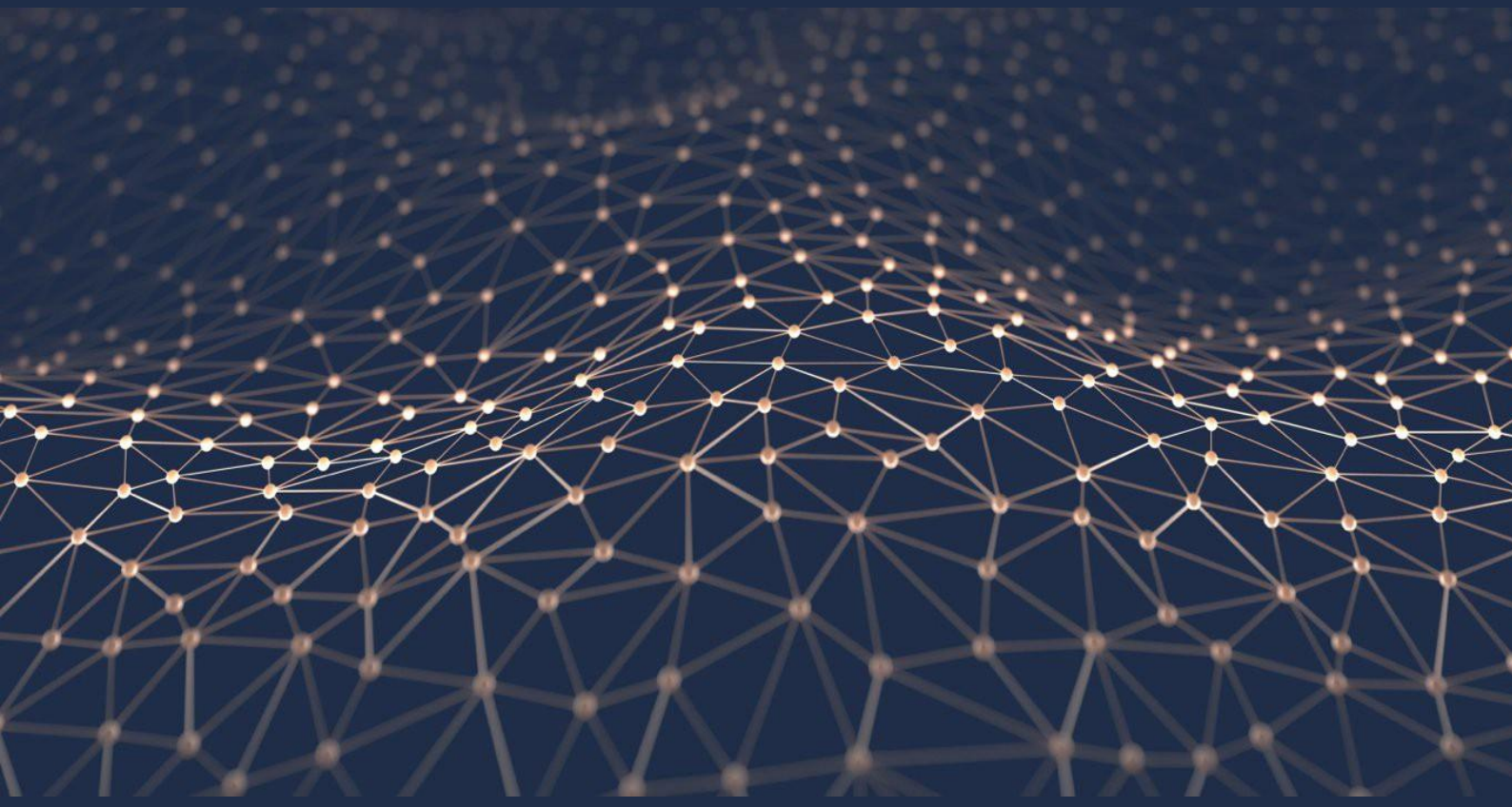
Deliverable D4.1:

Report on alternative technologies to k-NET for classification tasks



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1. Beneficiaries list:

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2. Project abstract:

Artificial neural networks represent a key component of neuro-inspired computing for non-Boolean computational tasks. They emulate the brain by using nonlinear elements acting as neurons that are interconnected through artificial synapses. However, such physical implementations face two major challenges. First, interconnectivity is often constrained because of limits in lithography techniques and circuit architecture design; connections are limited to 100s, compared with 10000s in the human brain. Second, changing the weight of these individual interconnects dynamically requires additional memory elements attached to these links.

Here, we propose an innovative architecture to circumvent these issues. It is based on the idea that dynamical hyperconnectivity can be implemented not in real space but in reciprocal or k-space. To demonstrate this novel approach, we have selected ferromagnetic nanostructures in which populations of spin waves – the elementary excitations – play the role of neurons. The key feature of magnetization dynamics is its strong nonlinearity, which, when coupled with external stimuli like applied fields and currents, translates into two useful features: (i) nonlinear interactions through exchange and dipole dipole interactions couple potentially all spin wave modes together, thereby creating high connectivity; (ii) the strength of the coupling depends on the population of each k mode, thereby allowing for synaptic weights to be modified dynamically. The breakthrough concept here is that real-space interconnections are not necessary to achieve hyper-connectivity or reconfigurable synaptic weights.

The final goal is to provide a proof-of-concept of a k-space neural network based on interacting spin waves in low-loss materials such as yttrium iron garnet (YIG). The relevant spin wave eigenmodes are in the GHz range and can be accessed by microwave fields and spin-orbit torques to achieve k-space Neural computation with magnEtic excitations.

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3. Purpose of the document:

The k-NET project proposes a new architecture for the realization of neural networks for neuromorphic computing and artificial intelligence by the operation in wavevector k-space. This drastically enhances the systems interconnectivity while minimizing physical circuitry and energy consumption of the neuromorphic hardware architecture. The radical new approach of k-NET will also have implications on algorithms where neuromorphic computing is used for machine learning and classification tasks such as vowel or image recognition. Prior to any benchmarking, as a nascent approach at an early stage of the k-NET project, a survey on alternative technologies for the neuromorphic hardware and the respective classification tasks is necessary. In this report, we thus present a state-of-the art survey of alternative technologies, their physics, and their application for neuromorphic algorithms for classification tasks. This sets the foundation for a sound estimation of the k-NET conjuncture for classification tasks in the following course of the project.

This document is related to the Task 4.1: "Choose and Study" which has the objective to identify the "place" of our technology in the landscape of neuromorphic applications, with a particular focus on object classification.

4. General introduction to neuromorphic computing

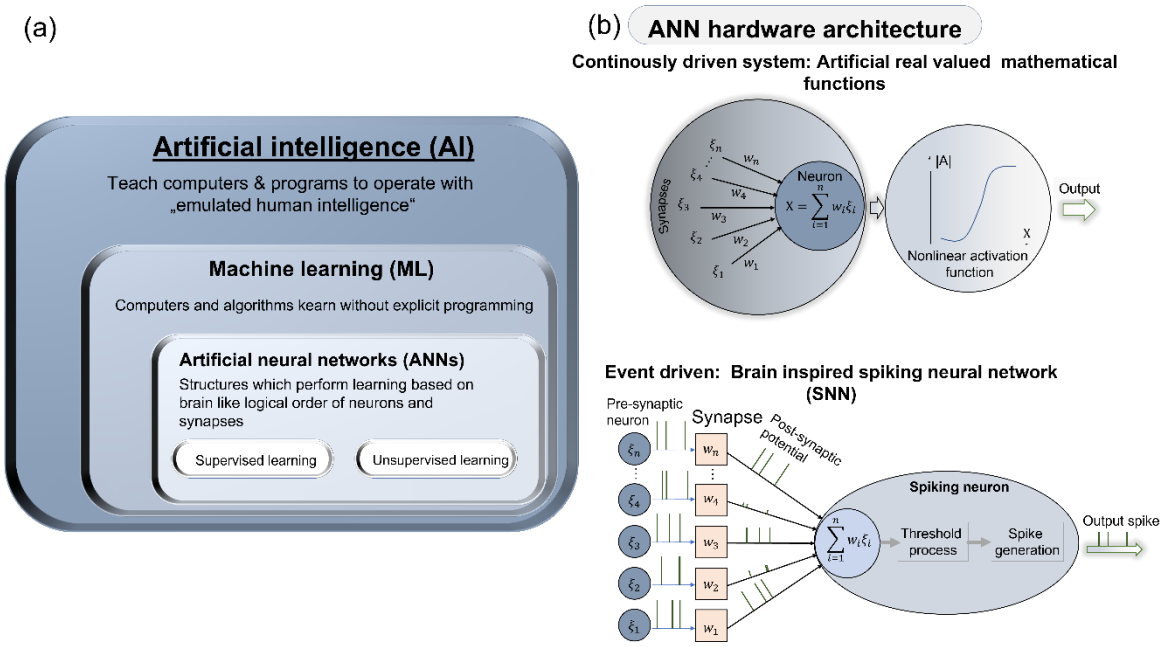

Figure 1: General overview: *Artificial neural networks as a subset of machine learning and artificial intelligence, respectively.* ***(a)****.* ***(b)*** *Current two main hardware architectures:* ***Top:*** *Type of artificial neural networks (ANN) emulating neurons by real-valued mathematical functions using nonlinear-activation functions towards the output, continuously driven and mostly in forms of. multi-layer perceptrons (deep neural network) employing hidden layers. Backbone of training methods for applications such as pattern classification and speech recognition using supervised techniques such as backpropagation methods. Usually implements with von-Neumann platforms (e.g., GPU etc.).* ***Bottom:*** *Brain inspired networks for artificial intelligence: Spiking neural networks (SNN)(a)-(b) adapted from V. Milo et al., Mat.* ***13****, 166 (2020) (c) Adapted from S. Dutta et al., Front. Neurosci.* ***14****, 634 (2020)*

The fourth industrial revolution towards an industrialized society 4.0 is in full swing and is going to introduce yet another paradigm shift in the way, we live, work, trade and communicate. Inextricably linked to this transformation is an exponentially growing demand for data storage, communication and

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information processing capabilities. If the requested demands should be provided by technology using CMOS based and classical von Neumann architectures, it is envisioned to exceed the global energy production by 2040 [1]. Thus, new means to satisfy the growing data demand while simultaneously facing the consequences of global warming and hence ways to minimize the global CO_2 footprint of the future technologies, are necessary. At the core of the industry 4.0, is the utilisation of artificial intelligence (AI) for optimization, intelligent, self-learning connection of machines, processes & production which not only employs state-of the art means of information and communication technology but also shapes the way we treat data and communicate itself. Although it is still under investigation by neuroscientists, the human brain is the best-known computation unit in terms of speed, energy efficiency, memory learning and optimization capabilities. Thus, key to artificial intelligence are approaches which aim to "emulate" the human brain via physical neuromorphic hardware implementations and "simulate" the learning and optimization via dedicated algorithms (depending on the specific choice of hardware). Up to date, classical digital computation and mostly the basis of current most mature AI system uses traditional artificial neural networks (ANN) (**c.f. Figure 1(a)-(b)**).

For instance, ANN have been shown [2]–[4] to be well suited for efficient data driven modelling tools widely used for nonlinear system dynamic modelling and identification. However, the human brain does not use bits for computing operations and deterministic data transmission but employs neurons and likely transmits in a nonlinear manner the data via stochastic spikes – short, voltage-based increases above a certain threshold ("*leaky integrate and fire operation").* These spikes are transmitted to other neurons via thousands of synapses. Then, the receiving neuron processes the input information (sum of charges from each spike) in a weighted sum operation, where each synapse carries its own synaptic weight to the desired output, forming a spiking neural network (SNN) (**cf. Figure 1 (c)**). However, memory and processor are not physically separated in the brain, thus not suffering from the inevitable hurdle of classical digital computation, the "von-Neumann Bottleneck"[5] (separation between memory and processing unit in von-Neumann architectures=modern computers), drastically increasing the energy for inference and learning processes. Thus, one core advantage of neuromorphic computing is the ultra-low energy consumption, and any type of existing hardware implementation seeks to implement the neuron & related correlations via different means of physical systems and principles. Correspondingly, the neuromorphic hardware implementations are then used to run suited algorithms for learning and applications such as image and speech recognition, natural language processing and nonlinear ways to learn, hence perform classification tasks. Hence, the main goal is the physical emulation of neurons and synapses at the small circuit or device level.

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5. k-NET: Approach

The approach utilized in k-NET is radically breaking with all previous approaches and establishes a new paradigm in physical neuromorphic computing in contrast to software-based approaches and therefore in AI. The disruptive, innovative approach lays in transferring neuromorphic computational operations from the real space into reciprocal, wavevector k-space. As will be detailed out later, this means immediately surpassing the von-Neumann bottleneck as memory and processing will be united in a single device via the achieved hyperconnectivity & reconfigurable synaptic weights. In k-NET the neurons are represented by – due to the geometrical confinement in nanoscale structures- discrete spin wave modes. Spin waves are low-energy collective eigen-excitations of (ferro-) magnetically thin films from the magnetic ground state at equilibrium. Hyperconnectivity is achieved by controlling the individual population (synaptic weight) of each mode via a mutual coupling exploiting nonlinear interactions (dipole-dipole mainly and exchange) serving as the synapses. Not only this means a significant decrease in size and, thus, increase in neuronal network density but also enhanced operational speed, dynamic control whilst requiring a hitherto unachieved minimal number of physical interconnections. The latter not only A. fasten up computation, but B. also will also drastically minimize the system's power consumption. Note, that **k-NET could be realised as a "traditional" deep neural network by utilizing the plethora of nonlinear interactions** between discrete spin wave k- modes. Operating in the nonlinear regime and in reciprocal space, in the hidden layers between the input and output layer as in a DNN, k-NET allows to directly feed the output of one neuron to the next one similarly to a recurrent neural network the individual neurons can experience direct or indirect feedback by the spin wave interactions in the nonlinear regime [6] . In the envisioned model of computing, where neurons are oscillatory modes, all to all interconnections come for free, from the physics of the problem. There is for instance no need to read out intermediate stage neurons. *Moving up to k-space architectures allows to solve the standing issue of connectivity.*

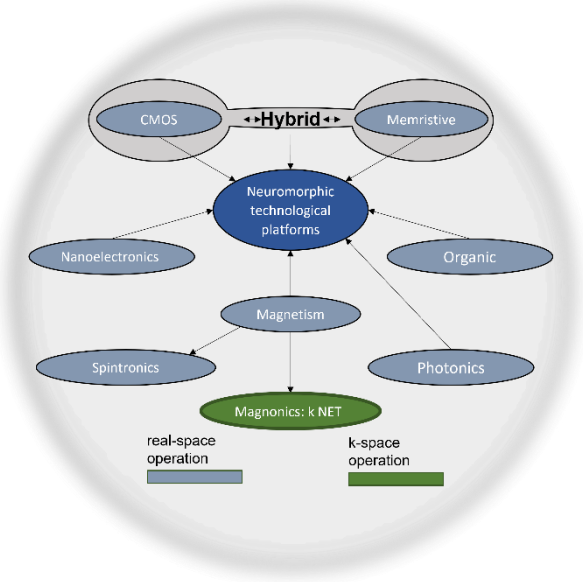

Figure 2: Overview on the different approaches for hardware implementations based on different physical systems for neuromorphic computing. *CMOS, memristor and CMOS-memristor hybrid technologies are technologically most mature are limited to the increasingly data hungry world: Limited by von-Neumann bottleneck (processing speed), size and power consumption. Other technologies (bottom) are emerging technologies, subject to fundamental research and mostly on small scales. Scalability is one main current issue. As a new technology k-NET is placed there but unique to all others due to the envisioned operation in reciprocal (k) space.*

Indeed, to date, the 3D connectivity of the neurons in the mammalian brain out of reach. A neuron in human brain is connected, on average, to 10^4 other neurons, which is unrealizable by current micro and nanoelectronics fabrication processes (that have at most 2.5 dimensionality) [7]. Attempts to build analogue neuromorphic hardware that required high interconnectivity were widely regarded as failed attempts such as the historical Intel ETANN chip from the early 1990ies [8].

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k-NET attempts to solve this decades-old problem by creating virtual interconnections between oscillatory eigenmodes, in lieu of the (unrealizable) physical interconnections. The interconnections are realized by inherent nonlinear interactions between oscillatory modes of the magnet. The 'neurons' of the device are the oscillatory eigenmodes, their amplitude and phase representing the analogue information.

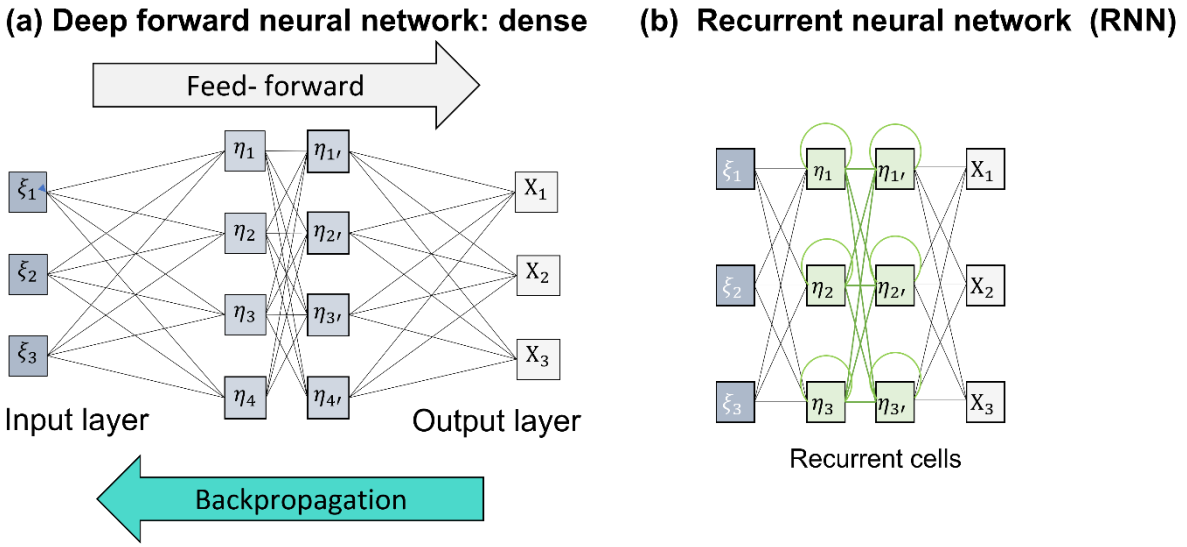

Figure 3 Schematics of the layers and connectivity for deep forward neural networks (a) and recurrent neural networks (b). *A forward deep neural network follows a one-way propagation path from the input to the output layer. If error correction is included Backpropagation methods are used to update the input and increase the system's learning accuracy. Typically, all neurons are fully connected, hence the network is "dense". (b) In a recurrent network there is not only a feed-forward propagation but the neurons in the intermediate layer can exhibit direct feedback to themselves or indirectly to neurons in the same layer.*

As eigenstates of the Hamiltonian, low-amplitude excitation modes of a nanomagnet are orthogonal and their time evolution is independent of each other. At higher amplitude this is no longer the case and the modes couple to each other, exchanging energy. Hence, that system is an- considering different scattering cross-sections between different modes inherently provides all-to-all coupling scheme, which is sought after in neuromorphic architectures. The system's connectivity is expected to be much larger than in physically wired systems. The strength of the couplings can be controlled by external microwave fields and / or the geometry of the system. The program (i.e. the weights between the neurons) is could be provided by the population levels of different spin wave modes or by the external field sequence. However, despite the clear advantages & innovative approach of k-NET, the core of k-NET relies on the largely unexplored physics of nonlinear interactions and couplings of magnons. Generally, spin based approaches that is spintronics and magnonics is now at the verge to technological maturity [9]–[11]. In view of the final goal of k-NET, the realization of a technological readiness level (TRL) **TRL 3 demonstrators** showing the basic functions of a neuronal network operating in reciprocal space it is inevitable to compare the individual aspects of k-NET such as challenges and advantages to the other approaches. *First*, that includes to identify the areas and -if existing- algorithms which need to be reshaped for specific use in k-NET or where more theory is required. *Second*, it implies to identify, where **k-NET** can be placed into the current landscape of existing technologies and approaches under investigation as well both from research and industrial institutions. **Such classification of alternatives technologies compared to k-NET is the objective of the first deliverable D4.1 of work package WP4.**

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5.1. Entanglement between Hardware and Software development for AI and neuromorphic computing

k-NET represents a fundamentally novel concept for hardware implementation and- at this stage- the demonstration of the k-NET conjuncture itself already represents a major scientific and technological breakthrough. A part of the objective is designated to the description of existing algorithms which are typically used for classification tasks, mostly using CMOS based technology. This will allow for an evaluation of best suited algorithms in k-space for k-NET since software and hardware cannot be separated in the same way as it is done in conventional neural networks. Additionally, among k-NET objectives is the development of *novel concepts of protocols for inference and learning shaped to the operation in k-space*. As described above, operating a k-NET device requires the design of field sequences that implement a certain computing task. Each computing task consists of three steps which are:

(1) initialization

(2) computing with all-to-all couplings

(3) readout.

Step (1) may use a multitude of input frequencies to initialize the modes, and (3) to read out mode amplitudes and phases. The fields of the (2) computing step are the ones realizing a fully connected network between the magnon modes. Referring to this, the design of the (2) control fields is a central challenge of the k-NET program. Currently, there are two **methods being pursued for designing this field sequence.**

The first approach is a blind, machine-learning based method that uses backpropagation through time (BPTT) for designing a field sequence for classification tasks. The input waveform to be recognized and the programming waveform is applied on two separate waveguides – the programming field is designed in such a way that when it is jointly applied with the input waveform, the output state of the magnet classifies the input.

The second approach intends to discover the physics of the nonlinear mode interactions and use this knowledge to design programming field sequences. For example, by using dynamic mode decomposition based on the results of micromagnetic simulations, we attempt to characterize the energy exchange between nodes and design the field sequences that map to a standard neural network. Additionally, it is possible to exactly write magnetization dynamics in a form of a series, which gives another tool for qualitative understanding.

Notably, the approach we take in k-NET is reminiscent of a quantum computing algorithm. In quantum computing (QC) models an exponentially large number of internal states is initialized, evolved and read-out to yield 'exponential parallelism'. While there are no exponentially numerous internal states in k-NET, the idea of parallel manipulation of large number of coupled internal states is closely related to QC. Quantum-inspired classical computing is now an emerging field and k-NET could be an important contender there [12]–[14].

However, given the current state-of-the art, the focus is now on the hardware to "emulate neurons and synapses." which is introduced by giving an overview on currently pursued physical platforms for realizing neuromorphic computing for AI.

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6. Overview state-of-the art neuromorphic hardware implementations: general remarks

To date, there exist various types of hardware realizations of neuromorphic computing which all have- when compared to each other- advantages, disadvantages and might be suited for one specific purpose in AI – depending on the desired application- better suited than the other (**c.f. Figure 2)** These individual approaches will be discussed in the following to allow a comparison of classification task from the alternative technologies compared to k-NET. That allows to place this new technology within the landscape of state-of-the art approaches under investigation.

As mentioned in the introduction, there are two types of neural networks. The "classical" artificial neural networks (ANN) operate in a continuous manner (input and output). In artificial neural networks the activation function of a neuron needs to be nonlinear and the neuron itself is represented by a mathematical function mapped to their real valued input [15]. Generally, ANNs are fully connected and usually realized in form of deep neural networks (DNN, **Figure3 (a)) also known as multilayer perceptrons** [16]. DNNs employ artificially constructed neurons based on nonlinear multi-valued (mathematical) activation functions which are applied to inputs in real space. The corresponding artificial synapses control the flow and direction of information in weighted sum operations representing the computational process when transmitted between neurons from one layer to another one (processing stage). That is, a deep network contains several intermediate layers between the input and the output level. These "hidden" layers allow, for instance, to decrease the dimensionality of the data from the input to the output level such as done in the case of image recognition, where only the desired image is given at the output [3]. Typically, the neuromorphic operations are fed forward from layer until reaching the output but there is no feedback to individual or between neurons. If the specific output of one neuron is connected to its own input, or to the input of a neuron from a previous layer , that is if there does exist such feedback, one refers to **direct and indirect recurrent neural networks**, respectively being closer to the human way of data processing [6], [17].

Instead, if an input layer is mapped to a high-dimensional space, the reservoir, in which dynamics of physical systems are used to process the information to the output layer. Typically, the reservoir remains fixed and the outputs from that high-dimensional physical states is trained. In turn, that renders learning in neural networks based on reservoir computing fast and simple learning such as classification remains simple and, consequently consumes much less energy (**cf. Figure 6 (c)**) [18], [19].

Furthermore, the existence and the realization of a dense network of neuron and synapses needs to be complemented with suited learning rules and training algorithms [20]–[22]. Accordingly, when a neural network is set to solve a task such as image recognition it follows algorithms with either a known input and error backpropagation methods (supervised learning) or an unknown input exploiting clustering effect via Hebbian learning (unsupervised learning). During that process, the network undergoes an inference phase computing the (first) output depending on the (given) input before it enters the training phase until the required accuracy is reached. Although these systems boosted AI and nowadays deep learning networks with algorithms with unprecedented accuracy (>99% exist [23], [24]), they exhibit complex and dense circuitry due to the number of physical connections. Among these approaches one can place CMOS, CMOS-memristive hybrids and artificial neural networks which are based on Photonics [25]. The information flow is still based on electrical current, which implies all drawbacks of involvement of electronic charge such as Joule heating, as compared to spintronic based approaches (**c.f. Figure 6 and references therein)** [26], [27]. In addition, traditional ANNs do not mimic the brain's functionality since- as previously mentioned- the brain does not encode information

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deterministically but rather use stochastic spikes to transmit the information [7]. Deep neural networks realized in classical von-Neumann computers are highly energy inefficient whereas brain-inspired, spiked Neural networks, can run much more energy efficiently and consume much less energy (10^{11} spiking neurons in the brain required 30 W compared a factor 1000x more to the same number of transistors in a supercomputer) [7]

The second class of systems and the respective hardware emulations are spiking neural networks (SNN) which indeed seek to function as the brain, using time-dependent gating of spikes such as via voltages [7], [15], [28]. They are envisioned to be more powerful and consume less power but suffer from lower learning accuracy as will be detailed out later.

Models such as "spike-dependent plasticity (STDP)" and feedback-based modulation techniques have been established in the past decade using leaky integrate and fire neurons. These types of neurons are comprised of a leaky capacitor in its simplest form, summing up the current from the synapses. The synapses are based on a threshold modulation of a physical effect **(as for k-NET**) to modulate the synaptic weight accordingly to the threshold modulation.

Spike based neural network (SNN) computing allows to simplify the related neuromorphic hardware implementations and consume only energy during the short time window of the spike activation [7], [28], [29]. In addition, natural synapses & neurons exhibit a plethora of functionalities beyond the spiking behaviour such as their stochasticity**,** leaky memories and integrators respectively[7], [15], [23]. Moreover, SNNs can show oscillatory and the possibility of synchronized behaviours. The latter, if implemented into physical systems can augment ANN and AI to the next level in the realm of the industry 4.0.

In this regard there is high interest in the implementation of SNNs which are truly brain inspired and there are various approaches. Among these approaches are spiking CMOS-memristor systems using non-volatile memory systems as mentioned above (True North Chip from Intel[30], Spinnaker Project of the EU Human brain project for edge computing and internet of things (IOT) [21], [31]–[33]) which is technologically most mature now. However, SNNs still need to exceed the performance from traditional DNNs and learning algorithms which equivalent as backpropagation algorithms from deep learning[29]. Furthermore, there are spintronic, oxide and 2DEG based approaches as well as detailed out below.

In general, the technological approach with the highest level of maturity are pure CMOS and CMOS-hybrid systems., mostly based on ANNs. The latter frequently use voltage-control on information transmission (synapses) via resistive switching also known as memristor devices. (RRAM, oxide based memristors) or photonics-based ones (c.f. **Figure 4 & 5)**. However, they suffer from drawbacks such as high energy consumption and bulky (cf. Spinnaker and BrainscaleS realizations) for the first or lateral sizes cannot be decreased below the optical wavelength (~1 µm) for the latter [15]. For instance, an event driven CMOS-neuron uses 9 µA for total bias current and consumes 40 fJ/spike/synapse [23], [34].

We believe that k-NET devices are most straightforwardly compatible with supervised learning tasks, albeit the learning algorithm will require 'conventional' external circuitry or software-based algorithms to tune programming field sequences. It is envisioned, that the strength of a given mode coupling could change continuously, with mode amplitudes and phases, allowing the straightforward use of backpropagation methods - or possibly with a different type of machine learning algorithm. An important goal of k-NET is developing a model of nonlinear mode coupling that enables efficient learning algorithms.

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6.1. Description of neuromorphic neural networks based on CMOS technology

Complementary metal-oxide semiconductor (CMOS) technology is the technological basis for today's communication and information processing. For decades it was fuelled by the continuous miniaturization of metal-oxide semiconductor transistors (MOS, Moore's law) until today joule heating and leakage currents do not allow for further miniaturization. Additionally, in computers, the memory and the processing unit are physically separated which limits information processing and computation speed, known as the 'von-Neumann' bottleneck (cf. [5] for instance) . One solution is to employ in-memory computing (c.f. [16]), which has been already applied to pattern classification [35], [36] or analogue image processing [37] and it is also applicable to neuromorphic computing applications based on CMOS. The implementation of DNNs and SNNs can for instance, allow for more energy-efficient in-memory computing and high scalability.

Among others, the foundation of CMOS based neural networks are memory transistors which form the basis for non-volatile storage applications. They consist of mainstream MOS transistors [16] which can accommodate a charge-storage layer within the gate which can be implemented in form of NAND [38] or NOR flash architectures [39]. The stored charge can be tuned by well-established Fowler-Nordheim tunnelling for program and delete and channel hot electron injection (CHEI) for program operations only. However, the program and delete process is limited to $< 10^5$ operations. Whilst NAND is suited for large data storage for the cost of long processing times (~µs), NOR flash technology is fast but only suited for small data packets. The subthreshold regime of an n-channel floating-gate memory and related variation of the device threshold voltage (synaptic weight tuneability) can be used to emulate the synaptic behaviour and, hence, for neuromorphic computing with CMOS technology. The synaptic transistor includes an additional contact to overcome a 'standard block-erase' scheme. In combination with deliberately rerouting standard NOR Flash memory single-cell selective erase operations can be enabled while keeping the overall cell structure unaltered as shown with 180 nm technology (Silicon Storage Technology) technology NOR arrays [40]–[43]. Although promising for ANNs, the statistical nature of the electron injection in the floating gate in NOR flash memory in the program phase leads to program noise. In combination with random telegraph noise from variation in the threshold voltage due to tunnel-oxide defects, the finite tuning precision of the threshold is problematic for DNN inference and limits also the system's stability in the offline training phase. To this end, that instabilities limit the system's scalability and classification accuracy.

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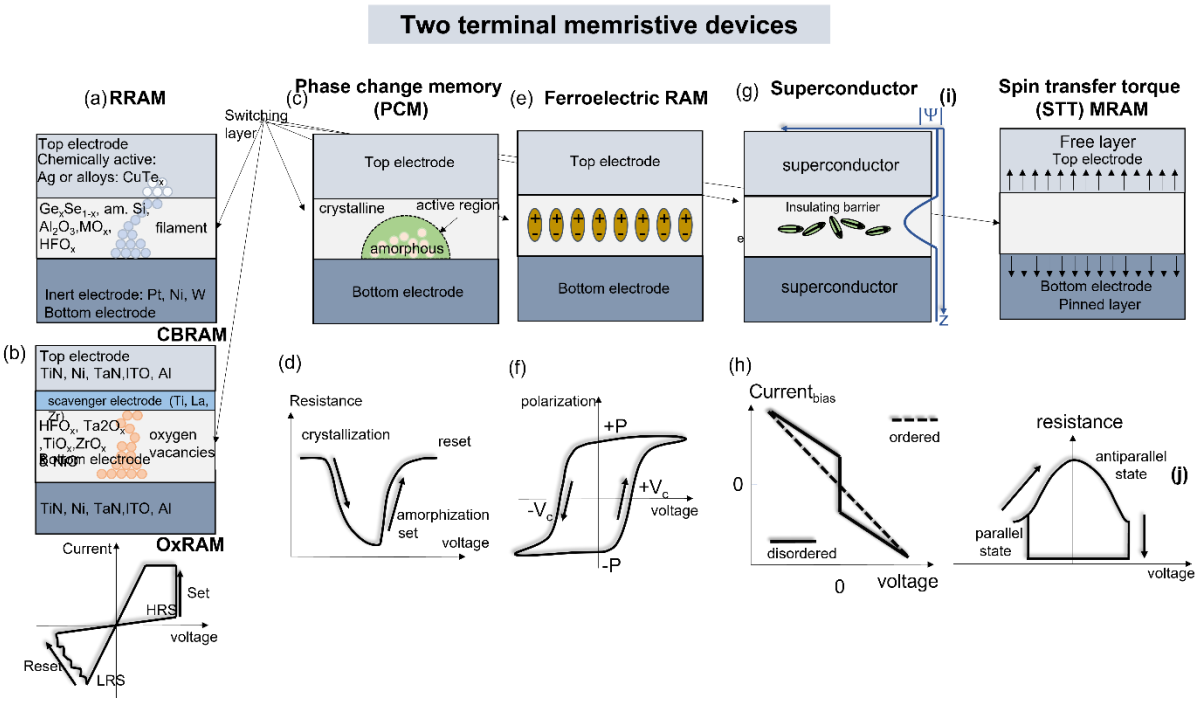

Figure 4 Overview on the individual approaches for non-volatile memory (memristive) approaches, often employed in a hybrid system together with CMOS based architectures*. I (a)- (h) display the schematics of physical principles and the current-voltage characteristics for common two-terminal memristive devices. These are conductive bridge or oxide resistive Random-access Memory (RRAM) where the resistance state depends on the formation of a filament. For Phase Change Memory (c, d) the resistance depends on the size of the crystalized volume and the amorphous region, whilst ferroelectric RAM (e, f) depends on the polarization of the electric dipoles. In Superconducting systems with a magnetic Josephson Junction, the resistance depends on the degree of magnetic order within the barrier. For the STT-RAM (i, j) a tunnel layer is sandwiched between the free and the pinned layer, the resistance depends on the relative spin alignment of the magnetic layers. Figure adapted from Ref. [11], [29], [48].*

For machine learning application, the traditional algorithms run on central processing units (CPUs), graphical processing units (GPUs)- mostly used for DNNs-, field programmable gate arrays (FPGAs) and, recently, on digital or mixed signal application specific integrated circuits (ASICs).

Using the third generation of artificial neuron models, SNNs, neuromorphic systems based on CMOS have been implemented by various research projects and international companies such as SpiNNaker from the University of Manchester, TrueNorth from IBM, Loihi from Intel,or BrainScaleS from Heidelberg University (c.f**. Table 1** and [44] and references therein).

6.2. Memristive:

Nanoscale, resistive memory (“memristive”) devices are another emerging class which is well suited for neuromorphic computing using SNNs. These devices employ non-volatile memory storage, and the information is stored in their system’s specific resistive or conductance state. As shown in **Figure 4** there are different types of memristors with different physical mechanisms for changing the resistance state such as phase transitions [**Figure 4 I (c)**] or spintronic effects **[Figure 4 I (i)],** and hence different current-voltage characteristics (**Figure 4 I (b, d, f, h)).** Additional to the tuneable resistance, memristive devices employ accumulative behaviour with a continuous increase or decrease of the associated resistance. The typical arrangement of memristive neuromorphic hardware in form of crossbar arrays [16], [34], [45], allows to achieve synaptic efficacy and plasticity such as spike -timing dependent plasticity (STDP, [46]). Synaptic efficacy describes the strength of the of input (presynapse) to influence

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the output (post-synapse) whereas synaptic plasticity refers to modulations of the synaptic weights during operation (execution of the learning algorithm) of the ANN [47].

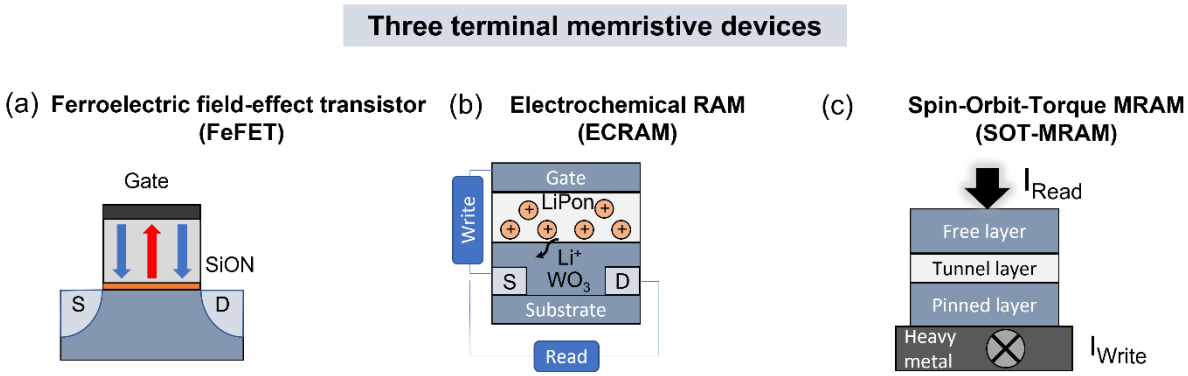

Figure 5: Three terminal memristive devices: *It displays the schematics of II(a) the ferroelectric field-effect transistor where the threshold voltage of the transistor is modulated by the ferroelectric switching II (b) Electrochemical RAM where the channel conductivity is controlled by ion (Li^+) migration and II (c) Spin-Orbit Torque RAM where the polarization switching in the free layer of the magnetic tunnel junction is induced by a current flowing in the heavy metal. Figure adapted from Ref. [11], [29], [48].*

Typically, non-volatile memory is ranging from RRAM (CBRAM, oxide RRAM: resistance change by filament formation) [23], spin-torque [26], [27] , phase-change RAM [48] or voltage-induced control of ferroelectric field effect transistors [49] . The necessary activation voltages are weighted by the conductance of the memristors. The resulting current is the sum from that weighed input.

In general, memristive device approaches can be divided into two- terminal and three-terminal devices (**c.f. Figure 4 and Figure 5)**. They are attractive to neuromorphic computing because of their capability of low-power operation, nanoscale site, analogue resistance technology and in-memory computing as well [16]. These systems have already demonstrated primitive cognitive tasks such as pattern recognition in neuromorphic networks [35], [50]–[52]. The two-terminal structure of RRAM, PCM, FeRAM or STT-RAM is similar. Between two metallic layers, also used as the top (TE) and a bottom electrode (BE) an insulating layer is stacked. The application of a voltage pulse induces a change of the physical properties in material of the switching layer. Hence, the corresponding physical property used to emulate the neuromorphic behaviour changes and to perform basic information processing by electrical operations on the memristive devices. Whilst the resistance is altered for RRAM and PCM & superconductor memristors, it is the electrical polarization for ferroelectric RAM and the magnetic polarization for STT-RAM (**cf. Figure 4 I (a, c, r, g, i)).**

RRAM relies on the formation and destruction of filaments to modulate the conductance. Depending on whether one uses a conductive bridge mechanism or an insulating oxide layer as switching layer, there are two types known as CBRAM or OXRAM, respectively. Further descriptions on the physical mechanisms can be found in the description of **Figure 4 in short** and extensively in Ref. [16], [23], [53]. As said, each architecture has specific advantages and drawbacks compared to each other. For instance, RRAM and PCM approaches employ dynamic ranges of programmable conductance states >100 (cf. [[16] and references therein) compared to 2-3 for STT-RAM devices but suffer from comparably low endurance. However, STT-RAM devices are envisioned to exhibit tremendously high endurance. On the circuit level wiring also limits the system's performance. Despite these drawbacks memristive synapses have potential for signal processing applications. For instance, using an SNN based on plastic PCM synapses and unsupervised learning temporal correlations could be detected [54].

Further, there are three-terminal memristive devices such as the ferroelectric field-effect transistor (FeFET), electrochemical RAM (ECRAM or spin-orbit torque (SOT) RAM (c.f. **Figure 5 (a)-(c)**). For

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instance, the FeFET approach allows to overcome constraints from the two-terminal FeRAM devices which can suffer from transient read currents and destructive read operations [16]. They were already implemented to memory arrays using 28 nm CMOS technology and are promising for 3D systems [16], [55], [56]. On the other hand, ECRAM were shown to operate in the nanosecond regime, which could substantially speed up training operations for ANNs whilst the decoupling of read/write current paths in SOT-RAM could enhance the endurance compared to spin-transfer-torque (STT)-RAM (cf. section on Spintronics).

However, all memristive approaches suffer from temporal, temperature-dependent variations in the conductance states and the nonlinearity and stochasticity related to the accumulative behaviours is problematic for up-scaling[57]. Additionally, note that memristors still employ Ohm's and Kirchhoff's laws which results in an enhanced circuit overhead. Thus, the energy consumption and area of the devices are increased as well. Correspondingly, that is disadvantageous in view of increasing demands for data storage, computational and processing capabilities the energy consumption needs to be minimized. Summarizing, no emerging memory device can unify all metrics of any neuromorphic network and its applications to date [16].

6.3. Hybrid CMOS-memristive systems

In CMOS-memristive hybrids, the synapses and respective neural network weights are stored in an array of non-volatile memory which are typically arranged in form of crossbar arrays and typically standard CMOS circuits (analogue or digital) serve as the "neurons".

Another common problem of both approaches is that despite being already commercially available in the case of the CMOS based systems and ultrafast operational speeds in the case of the photonic system, the size of the neurons is not translatable to the nanoscale and thus the density of the respective neural networks will remain sparse. The utilisation of hybrid CMOS non-volatile memory circuits, mainly memristor based currently suffers from **cell-to-cell variations** of the switching threshold which leads to variations of the synapses. Furthermore, typical RRAMS exhibit a relatively low resistance in the low resistance state (LRS) ~kΩ and high-power consumption in the CMOS driver circuits [58]. The resistance can also undergo **time dependent drifts** which are in themselves also temperature dependent and will lead to decrease the accuracy at the output. Apart from that, the number of write cycles is limited on such devices and hence these systems exhibit a limited **endurance** as well.

Thus, recently new approaches spanning fundamental research and technological maturity have been explored. These include hardware implementations employing photonics, spintronics (**c.f. Figure 6),** low-dimensional structures such as two-dimensional electron gases (2DEGs) (**c.f. Figure 7**) or even based on superconductivity (**c.f. Figure 4 (g), (h)**). Specifically, spintronics approaches, where the electronic spin instead of the electronic charge serves as the principal information carrier, can operate in the nanoscale but currently lack scalability towards large-scale implementations. Furthermore, existing implementations of spintronic neurons, and their interconnections, i.e., synapses, operate in real space using physical interconnections (**c.f. Figure 2**).

The neurons can be also mapped into different time delays if the time-delay architecture of reservoir computing is employed [59]. Hence, they require a careful design and structuring of the individual nonlinear elements. The latter does not only increase the systems complexity but limits the connectivity.

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This will be especially become problematic when future neuromorphic spintronic chips are about to be integrated into current CMOS networks and using algorithms running on conventional computers, i.e., von-Neumann architectures.

6.4. Description of neuromorphic neural networks based on photonics

Significantly faster than hybrid-CMOS systems are photonic networks employing optical nonlinearities such as the Kerr effect for the emulation of the neurons and for the synapses interferometrical & phase control methods [15], [60]–[62].

Photonic synapses can be implemented electrically controlled via waveguide interferometer meshes [61] or all optically via PCM based photonic synapses or amorphous metal-sulphide microfibres [63], [64]. On the other hand, photonic neurons can be realized by either electro-optical or all-optical means such as silicone photonic modulator neurons, superconducting optoelectronic neurons [65], [66]or again PCM based spiking neurons [60], respectively.

Although being ultra-fast in terms of operation due to the utilization of photons and the possibility to realize passive neural networks (minimizing again the energy consumption) this approach is limited by the minimal size associated to optical wavelengths. Also, optical systems are mostly 3D structures and challenging to realize them in a chip-scale device. Thus, they are not best suited for the application spaces pursued in k-NET but yet show great potential for computationally hard problems [25].

6.5. Description of neuromorphic neural networks based on spintronics

Spintronics, also known as spin electronics, uses the electronic spin and its associated magnetic moment as the central carrier for information processing. Though still a nascent market, spintronics is about to be implemented on a large industrial scale. For instance, spintronic based MRAM technology are progressively replacing DRAM memories [67] and- for instance- actively investigated for in-memory computing by companies such as Samsung [68]. Other possible applications of spintronics devices are in radiofrequency applications that may benefit from the physics of spin-transfer torque nano-oscillators (STNO), spin diodes, spin filters, devices based on giant- or tunnel- magnetoresistance or pin-transfer-torque devices. Spintronic devices exhibit almost unlimited endurance, non-volatile memory, and ultra-fast dynamics due to typical frequency ranges from GHz to THz for ferromagnets and antiferromagnets, respectively. The electronic spin also inherently has some similarity to constituents of neural networks [27].

Since flipping of one spin is a stochastic process it is naturally analogous to the stochasticity of the firing of spikes in the brain. Therefore spin-based electronic is not only most promising beyond- CMOS devices, spintronics is also highly promising for neuromorphic computing.

As displayed in **Figure 6,** there are various spintronic technologies for neuromorphic hardware and computing, which are currently investigated. These are, magnetic tunnel junctions (MTJs) (**Figure 6 (a)**), – very recently- antiferromagnets (**Figure 6 (b)**), spin-orbit-torque (**Figure 6 (c)**), skyrmions (**Figure 6 (d)**) and domain-wall propagation (**Figure 6 (e)**), where the latter three can also be classified as spintronic memristors. Among MTJs there are nano oscillators and superparamagnetic MTJs.

6.5.1. Magnetic tunnel junctions (MTJs)

In an MTJ a tunnelling layer is sandwiched between two ferromagnetic layers whose magnetization acts as a fixed and a free layer respectively. Additionally, to prevent undesired switching by exchange bias the fixed layer is usually coupled to antiferromagnetic layer. When the magnetization of the free

and fixed layer is parallel (antiparallel), the corresponding tunnelling magnetoresistance of the MTJs is low (high). The manipulation of the free layer can, for instance, be conducted by spin-transfer-torque (STT) where transfer of spin angular momentum occurs through the passage of a spin-polarized current. Apart from their endurance, MTJs exhibit high thermal stability, comparably good scalability and low readout time, which resulted in the – still ongoing- development of STT-MRAM[27]. There are spin-torque nanoscillators (A) and superparamagnetic MTJs (B)

A. Spin-torque Nanooscillator (STNO)

The spin dynamics of the free layer is governed by the Landau-Lifshitz--Gilbert-Slonczewski equation (LLGS) which describes damped precessional motion with spin-transfer torques [15], [69]**.** When a direct current is injected into an STNO, it can be driven to the auto-oscillation regime in which magnetization precesses continuously [70], [71]. This is due to the presence of a specific orientation of the STT which leads to an additional anti-damping torque which can balance the damping torque from the LLGS. STNOs exhibit a nonlinear voltage-current dependency and are highly tuneable in frequency, amplitude and electrically controllable. A STNO mimics the spiking behaviour of a biological neuron by generating periodic output voltages if periodically driven and the magnetic damping takes the role of the leaky behaviour of that neuron [26], [27].

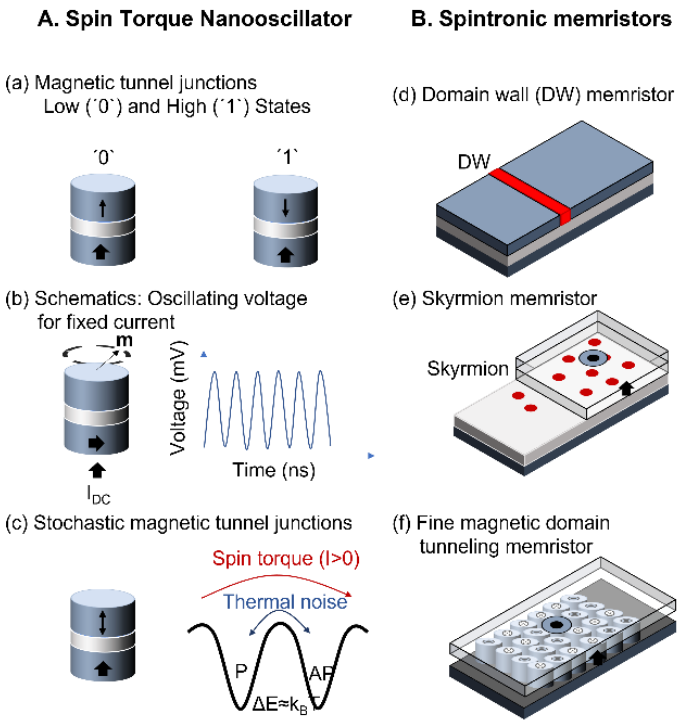

Figure 6 Overview on the spintronic based approaches*. A. Spin Torque Nanooscillator implementations where (a) shows magnetic tunnel junction. The resistance is high (low) in the antiparallel (parallel) state. (b) Nanooscillators (c) Stochastic magnetic tunnel junctions. B. Overview on memristors based on spintronics. (d) Concept of a domain wall memristor which can be moved by current, for instance, the skyrmion memristor (e) and (f) a fine magnetic domain tunnelling memristor. Adapted from Ref. [20]*

The biological neuron integrates the incoming signal with leakage and fires an outgoing spike when a certain threshold is reached, thus under a periodic drive it will fire periodically as well [72]. Additionally, under external microwave drives ([73], [74]) or mere proximity such as via direct exchange interactions [75]–[77], STNOs can enter synchronization with other STNOs and hence build the basis for upscaled neuromorphic networks [78], [79].

B. Superparamagnetic MTJs [80]–[85]

Recent results from neuroscience indicated the brain uses stochasticity in the biological neurons and synapses to reduce the brain's energy consumption [26], [79], [86]. Stochasticity allows to rapidly sample a large parameter space in order to find optimal solutions.

Thus, by decreasing the thickness of the free layer of the MTJ below the superparamagnetic limit such that the energy barrier between the parallel (RP) and antiparallel, Rap state is in the same order than the thermal energy. Thermal fluctuations induce transitions between the two states in the free layer (cf **Figure 6 (b)**) with equal probability. The application of an electric bias changes the switching

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probability and hence controls the firing as a Poisson process- as in biological neurons [83]. Hence superparamagnetic MTJs allow for the realization of low-energy neurons.

6.5.2. Antiferromagnets

Collinear antiferromagnets are characterized by the antiparallel alignment of neighbouring spins in a magnetically ordered material due to the negative sign of the Heisenberg exchange constant. Similarly, to ferromagnets, antiferromagnets can be manipulated via SOT but operate at much higher frequencies (~THz). Furthermore, given the antiparallel alignment of the spins, antiferromagnetic systems are much more robust against perturbation with external fields. The antiparallel alignment of neighbouring spins results in a zero net magnetization and hence vanishing stray fields which would supress magnetic crosstalk in densely packed structures in the future and yields higher scalability. However, this approach is much at its infancy and is currently hindered by the low readout signal. Most mature are currently AM/FM heterostructures which induces memristive behaviour via exchange bias in the ferromagnet.

6.5.3. Spin-orbit torque (SOT) [87]–[89]

Spin Orbit Torque originates from the coupling between the electronic spin and orbital angular momentum, also known as spin-orbit coupling. For instance, in a normal metal- ferromagnet bilayer system, a transverse electric current in the normal metal layer induces a net spin polarization (Spin-Hall-Effect) which exerts a torque on the ferromagnetic layer and can drive magnetization oscillations. The transverse current flow in the normal metal layer compared to current directly passing through the junctions as for devices based on STT, i.e., STNOs, SOT based systems are more versatile. They allow to consider new material classes such as oxides [94-96], 2D materials [97-99] for neuromorphic computing as well (cf. Section on lowdimensional materials).

Compared to STT driven devices, SOT based magnetization switching and their energy efficiency is envisioned to be higher, because of the magnetization switching is not limited by incubation times due to thermal fluctuations and the torque/electron is estimated to be higher, respectively [87]. Correspondingly, a spin Hall nano-oscillator (SHNO) is driven by the SOT. By synchronizing 2D arrays of mutually synchronized SHNOs, the connectivity can be improved [90]. However, this approach is still at its infancy compared to the other ones.

6.5.4. Skyrmions

Magnetic skyrmions are topological spin textures in a chiral magnet and can also be regarded as solitons. Similarly, to DW propagation, a skyrmion can be manipulated and moved by SOT. The nonlinear resistance changes in magnetic skyrmions upon motion for instance can be used for the implementation of skyrmionics memristors [91]–[93]. The particle-like nature and the thermal Brownian motion of skyrmions would allow to represent the spintronic implementation of the biological leaky integrate- and fire neurons. Although simulations demonstrate the resistance could be tuned by controlling the interplay between STTs and anisotropic magnetoresistance and use the output voltage for the implementation of skyrmionics synapses, experimental demonstration is currently lacking.

6.5.5. Domain wall propagation

A domain wall, which is an example of a one-dimensional magnetic soliton, separates magnetic domains – uniformly magnetized areas – in a magnetic material [26], [94]. . Spin currents can also move domain walls through spin-transfer-torque (transverse current leading to current-induced domain wall motion) or spin-orbit torque, while the domain wall position can translate to a variation of the device resistance. [95], [96]. Back and forth domain wall motion can be used as a memristor

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which is non-volatile with a high degree of plasticity [94], [97], [98]. Furthermore, as for skyrmions the depinning and motion of magnetic nanostructures is inherently stochastic and together with magnetic-domain wall-based logic can be used for neuromorphic computing.

6.6. Description of neuromorphic neural networks based on low dimensional devices

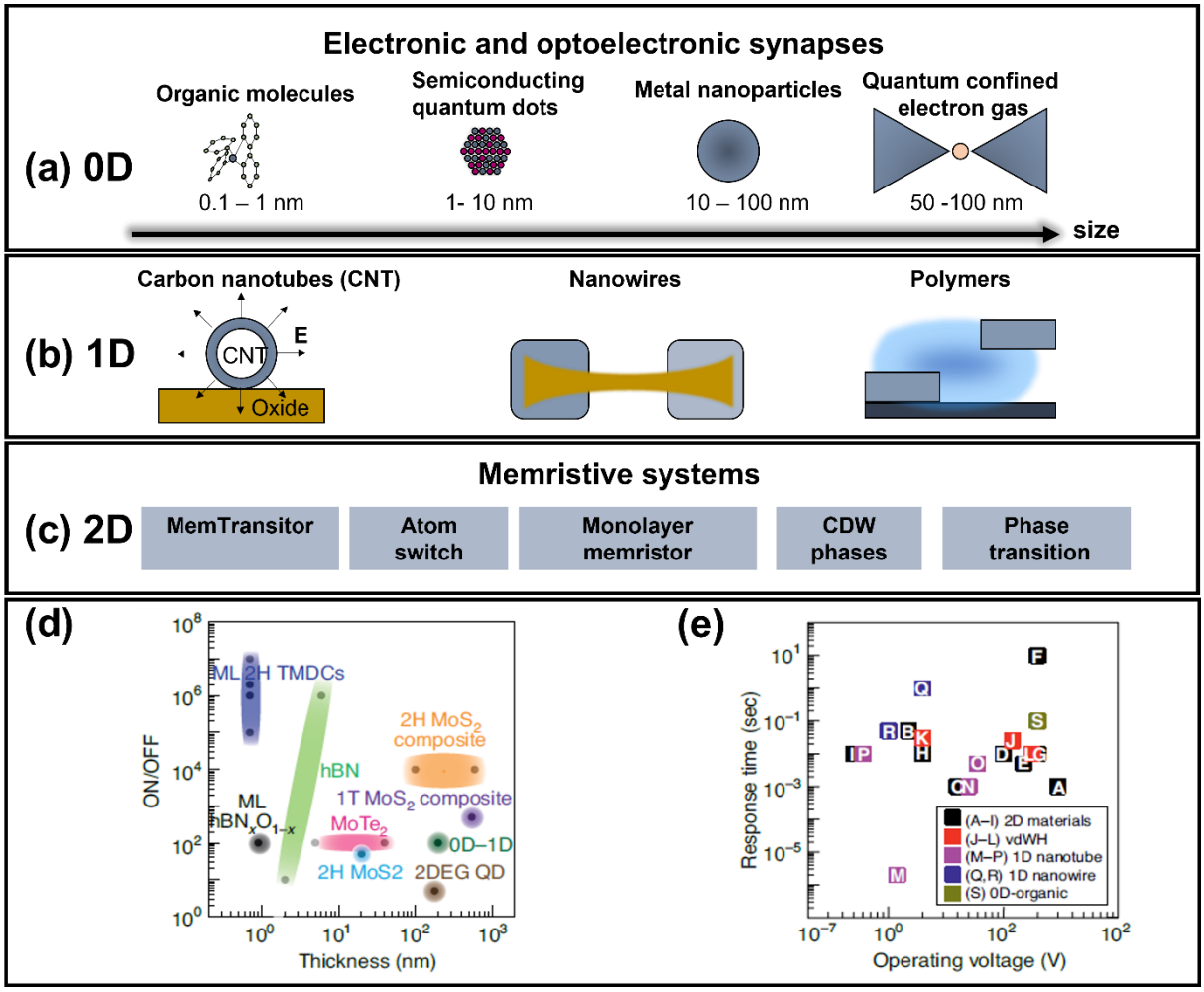

Figure 7 Overview over low-dimensional nanoelectronics' approaches for neuromorphic computing. (a) 0-Dimensional approaches which depending on the extension include organic molecules [99], semiconducting quantum dots [100], [101], metal nanoparticles [102] and quantum confined electron gases (e.g. [103]). (b) Overview on one dimensional (1D) approaches which include carbon nanotubes (c.f. [104]–[106]), nanowires [107], [108] or polymers [109] . (c) Overview on two-dimensional (2D) approaches, under which memtransistors [110], atomic switches [111], monolayer memristors [112], [113], CDW phases[114]] and phase transitions [115] belong to. (d)-(e) Comparison of all nanoelectronics' low-dimensional approaches for ON/OFF ratio and operating voltage, respectively from Ref. [20]. Figure adapted from Ref. [20] .

A new class of low-dimensional nanomaterials is comprised of zero-dimensional (0D), one-dimensional (1D) and two-dimensional (2D) approaches as shown in **Figure 7 (a)- (c).** Whilst the 0D and 1D nanomaterials allow highly sensitive functionalization and redox chemistry for multi-bit states 2D architectures can provide in-situ probing, spatiotemporal responses and a platform to implement multiple electrodes [110], [116], [117]. The lower dimensionality of such systems could also enable once wearable neuromorphic applications [118].

Due to their optical properties and controllability, 0D nanomaterials are well suited for neuromorphic implementations in photonic systems such as optoelectronic synapses. The utilization of photonic devices can enable the required parallelism and hyper-connectivity for ANNs. For networks, for

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instance 0D quantum dots are investigated due to their multi-band emission and 0D type memristors were realized, which are controlled by electrical and optical pulses [103], [119].

Based on QD arrays quantum neural networks or other neuromorphic architectures have been proposed as well. 1D structures are comprised of carbon nanotubes, nanowires or utilize polymers (**Figure 7 (b)**). For instance, it was demonstrated that depending on the choice of doping (p- or n-) of carbon nanotube thin-film transistors, it is possible to convert the relative timing information into pulse amplitudes which is relevant for an easier implementation of STDP [120]. The electronic properties of such systems are also highly sensitive to adsorbates and hence could be used for sensing in neuromorphic nanosystems [106]. Volatile and non-volatile, i.e., memristive behaviour, that is resistive switching was shown with nanowires which behave fairly like carbon nanotubes. They could be used to emulate the morphology of biological nerve fibres or biological ion channels [121]. Polymers have been employed for mechanically flexible nanoscales memristive systems [122].

2D approaches follow the standard memristor principle and can offer the integration with planar wafer technology with high switching ratios ($\sim 10^4$). Different approaches are listed in **Figure 7 (c)** for 2D. For instance, graphene-based synapses show tuneable plasticity. Synaptic transistors in black phosphorous, which is also a promising material for anisotropic synaptic response due to its in-plane electronic properties, were investigated as well [123]. 2D materials can be also used to realize memristive behaviour and transistors functionalities in one device which are usually not compatible and are also known as memtransistors by using separate layers [110].

The individual properties of all approaches can be found, for instance, in Ref. [20] and references therein for more details, but these are beyond the scope of this report. Nevertheless, **Figure 7 (c)** shows a state-of-the art comparison of the switching ratio vs. the channel thickness **(7 (d)-(e))** and of the response time vs. the operating voltage for synaptic transistor for low dimensional nanosystems, taken from Ref [20]. However, to date, most low dimensional approaches are at the level of fundamental research, i.e., proof-of-concept level, and hence will be not further mentioned in the discussion on classification tasks in the next section.

6.7. Other approaches: Organic materials

It is worth mentioning that there is also an emerging class of organic materials with a low energy consumption but can be also highly mechanically flexible. Furthermore, due to their organic nature they are biologically compatible. However, they are comparably slow during operation and suffer from a limited accuracy due to the instability of organic materials [99]. The reader may refer to numerous excellent reviews for further information on this approach, which is a research field in its own right. For instance, see for Ref. [124]–[127] and references therein.

6.8. Spin wave-based approaches such as k-NET: Assets of magnonics

Magnonic structures have unique benefits that distinguish them from other emerging approaches for neuromorphic devices. Broadly speaking there are three fundamental benefits:

1. Magnonic devices are highly interconnected, which was also a significant benefit of photonic device
2. Nonlinearities come for free in magnonic systems and appear already at moderate magnonic intensities
3. Magnons carry and process information at high speed while using low power.

Specifically, for (1) there are a number of devices that imitate optical computing models (cf. Ref. [128], [129]) and these devices do not require internal interconnections. Specifically, all operations can be performed in the magnonic domain. There exist as well design methods for building magnonic versions of optical device components [130].

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As for (2), magnonic behaviour starts to become nonlinear beyond a few degrees of precession angle, which is readily achieved in most device setups still at low power levels. This is in sharp contrast to optics, where typically high intensities are needed to show any nonlinearities. Nonlinearities are required for any non-trivial computation and are essential to neuromorphic devices.

Regarding (3), it is well known that in electronics on can often trade in speed for power, and low-power integrated circuits are slow by design. Magnonics is uniquely capable of low-power processing while maintaining high speed. Magnonic wave conduits can transmit information at Gbit rates, while consuming potentially well 1 eV transmitted bit [10]– such characteristics are unmatched by electronic systems.

For a more detailed benchmarking effort, see Ref. [131] and references therein. In general, magnonic devices fare well in these comparisons. An important message in Ref. [131] is that to benchmark neuromorphic hardware, one has to consider the cost of interconnections and overhead coming from device interconnections. In high-interconnected structures the energy cost of interconnections could be much higher than the cost of the neurons itself. This overhead does not necessarily appear in magnonic devices and does not appear in k-NET either.

6.8.1. Inverse-designed magnonic scatterers

Very recently it was shown that propagating spin waves can perform highly non-trivial classification tasks and that such nonlinear dynamic systems can be inverse-designed using machine learning methods [132].

The device proposed by Papp et. al. (Ref. [132]) uses nonlinear spin wave (magnon) interference to perform classification tasks. The waveform to be classified is applied to a waveguide and this waveguide launches propagating spin waves in a YIG film. The YIG film is patterned in such a way that the nonlinear spin wave scattering performs vowel classification – for example, the magnons are focused to particular areas in the film depending on what is the waveform (vowel) that was applied on the waveguide. The device of Papp et. al. uses propagating spin waves, not confined modes as targeted in k-NET. However, both systems use nonlinear magnon interactions to do classification. The successful application of machine-learning methods by Papp et. al. suggest that machine-learning is a viable route to train k-NET devices. Note that in general - despite the specific approaches and their advantages and disadvantages- a large scale integration of any neuromorphic hardware implementation on an industrial level requires high neuronal network densities and hyperconnectivity (>1000 synapses/neuron) to perform fundamental tasks in AI. The most advanced platforms are based on CMOS o CMOS/memristive hybrid systems but suffer from problems as detailed out such as being bulk and being still von-Neumann architectures.

6.8.2. k-NETs envisioned assets compared to other neuromorphic hardware implementations.

In small, confined geometries, spin wave (SW) modes become quantized and then only populate a discrete set of modes in reciprocal space (k-space). Hence, they exhibit a discrete set of resonance frequencies as well. In the picture of a harmonic oscillator and in the linear regime, each SW mode can be considered as an independent oscillator. However, if the system is driven into the nonlinear regime this independent behaviour is not valid anymore, and the system become highly coupled.

As said, magnonics, the research field associated to use magnons, i.e. the quanta of spin waves as central information carriers frequently employs the resonant energy absorption of the (for k ≠0, propagating) collective spin excitation at specific (magnetic) fields and frequencies for manipulation,

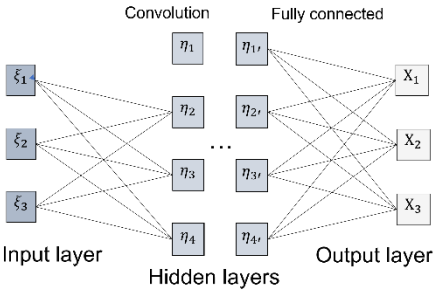
transport and read out of the information encoded in the SW modes [133]. Intrinsic nonlinear interactions in ferromagnetic systems couple the SW modes together. In the case of sufficiently large drives, i.e., deviations from the SWs ground state, these effective fields render the SW dynamics nonlinear.

The strength of the respective nonlinear interaction in k-space depends mostly on the SW amplitude, which is related to the population of a specific mode. Controlling the synaptic weight therefore involves controlling the population in the SW modes. That control can be obtained by transverse and parametric pumping with external magnetic fields, which can facilitate mode conversion through a number of different nonlinear processes. The inherent property to unify all oscillations and interactions (neurons & synapses) in a single entity, represents a great asset of the k-NET approach compared to previous approaches employing nonlinearities and multiplexed frequency inputs. The single entity of k-NET is a single resonator which means that the von-Neumann bottleneck can be immediately surpassed. No circuitry to make the link between neuron and synapse is required. The absence of additional circuitry is expected to simplify the system's complexity, size, energy consumption and operation speed as their connections required in real space operating approaches do not exist and thus do not slow down the computation process. Furthermore, as information is encoded in magnons and magnon currents, no joule heating from the neurons and synapses themselves is involved. The main dissipation will come from the employed radio frequency antennae but as there is only the need of few to achieve the drive, the circuitry is less dense than conventional CMOS, or CMOS-memristor or other comparable systems. Thus, operation at the nanoscale and of multiple dense neural networks is envisaged.

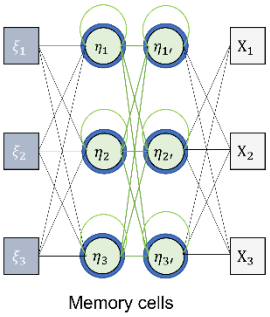
7. Technology comparison: Different approaches for classification tasks:

7.1. General introduction: Discussion on DNNs and SNNs for training and classification

(a) Convolutional neural networks: Sparse



(b) Long/Short Term Memory Network (LSTM)



(c) Reservoir computing architecture

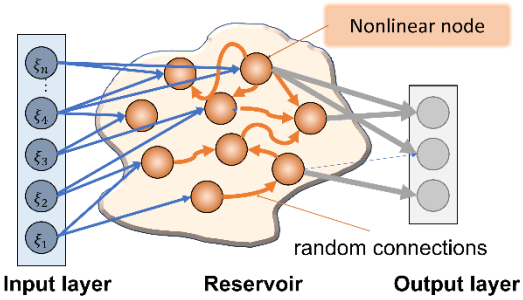


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Figure 8: Overview over other structures for learning and classification than only DNNs or RNNs (cf. Figure 3). *(a) Deep neural networks, fully connected with one or several hidden layers between the input and output (b) Convolutional neural networks (c) Recurrent neural networks (d) Long/Short Term Memory Networks (LSTM)(e) Principle of reservoir computing. An input layer is given to a reservoir where the system undergoes nonlinear interactions with several interconnections and outputs trained weights to the output layer.*

Broadly speaking, neuromorphic machine learning for classification tasks employs the training of the synaptic weights until the desired accuracy is reached.

Generally, the traditional deep learning techniques with using backpropagation show the highest classification accuracy but these networks are feed-forward networks, typically larger in size and slower due to the complexity of both the interconnections and the iterative error-reduction methods in backpropagation for complex models. Other methods for classification tasks are ones based on reservoir computing and on spiking (recurrent) neural networks. Whilst the first uses a pre-processing step to obtain linearly separable data via a recurrent reservoir, the second is also known as Evolutionary Optimization of neuromorphic Systems (EONS) where the recurrent spiking neuromorphic network systems are trained via specified algorithms. Deep learning algorithms include the Perceptron, the multi-layer perceptron, convolutional models such as Conv and LSTM (Long-Short Term Memory) **(c.f. Figure 8**). Perceptron based models are fully connected (dense). Compared to perceptrons with only two layers (input and output) multi-level perceptron networks are known to be good classifiers as they also employ multiple layers and nonlinear functions in the same time. Convolutional models were first developed for handwriting recognition and useful for different input forms [134]. However, for learning concerning higher dimensional features and time-series data, stacked layers with LSTM are better suited. On the other hand, training a spiking neural network aims to define the connections, thresholds, weights, and delays such that the classification task can be accomplished. That means that the collection of data points from a dataset their values must be converted into spikes and the output classifiable again. For instance, a Neuroscience Inspired Dynamic Architecture (NIDA) has successfully shown to be applicable to data control and classification [135], [136]. However, NIDA is dynamic, and backpropagation cannot be used. One solution is there using EONS which relays on updating fitness values from an initially randomly generated network by choosing the highest fitness values per iteration until a desired threshold is reached.

In general, classification applications originate from a plethora of field and algorithm from above is better suited for one specific application than the other. Most common ones are the MNIST (**M**odified **N**ational **Institute** of **S**tandards and **T**echnology) for handwritten digits recognition or the CIFAR-10 (Canadian Institute For Advanced Research) dataset with 60,000 32x32 colour images in 10 different classes for image classification [137]. Additionally, there are less used ones such as old **IRIS** (image recognition) dataset for flower recognition, **RADIO** dataset for training signal-to-noise ratios or datasets for consonant vs. vowel, i.e., speech recognition tasks such as **TIMIT**.

Discussion on SNN based learning for improved neuromorphic computation

In principle, SNNs are advantageous to mapping non-spiking AI algorithms to real systems but, to date, their main limitation to technological maturity is the lower classification accuracy after inference and learning steps. There are SNNs which are converted from trained ANNs using ANN-SNN conversion and there are direct SNNs which are derived from spike- based training. The first method which is also used by Intel's True North Chip and Spinnaker improved a lot the power efficiency compared to previous attempts, but the estimation of the spike rate required non-trivial passages of time [28], [29]. It has been proven, in fact, that spiking neurons are fundamentally *more powerful* computational units than traditional artificial neurons. However, one issue for SNNs is the implementation of efficient learning algorithms which are equivalent or outperform existing types of DNNs with backpropagation for error minimization and updates. Although for SNNs there exist unsupervised learning methods such as Hebbian learning and STDP, there are currently no supervised training methods for SNNs that

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outperform the second-generation non-event-driven networks. Spike trains are not differentiable, therefore typical gradient descent cannot be employed, either as one cannot maintain precise temporal information in spike trains. Therefore, to properly use SNNs for real-world classification and artificial intelligence, better supervised learning methods with higher classification accuracy need to be developed as well. Using the exact time of pulse occurrence, a neural network can **employ more information and offer better computing properties**. The SNN approach produces a binary output instead of the continuous output of traditional forward non-spiking DNNs (classical ANNs). The direct spike- based methods for training are either unsupervised methods with signals localized to one synapse such as Hebbian learning and STDP (Spike-Timing-Dependent Plasticity) for SNNs or optimization based, supervised ones. However, to date, supervised learning algorithms utilized in SNNs are much less accurate than, for instance, the well-established back-propagation methods from classical "ANNs" due to the errors in the weight-updates. Referring to the latter, this error originates from inherent noise in the employed nanodevices, and thus the weight- control and adjustment is aggravated. Another problem is that the current networks are rather shallow, less powerful and an extension to large scale might be difficult. For instance, a current state-of the are direct spike-based example achieves 95% classification accuracy on a MNIST dataset[138] a STDP two-layer network with 6400 output neurons which is still lower than classical ANN models with standard backpropagation methods ([139] pp. 318-362). However, recent works show improvement from that side as well, such as using a "gradient based inference method" to achieve up to 99.59% accuracy for a MINST dataset. When the same algorithm is applied to other datasets for classification tasks such as SVHN or CIFAR-10 (both used for image recognition) it is close to other approaches which use ANN-SNN systems for instance [138], [140] or spatiotemporal backpropagation [141]. Compared to the classical approach it is only 0.5-1.5 % lower now [28], [142]. Additionally, one way to overcome some issues of above learning, would be to allow the learning with the imperfect, dynamical and noisy nanodevices at hand, that is to allow for unsupervised learning as there the information flow is highly unconstrained. Hence, it is less sensitive to system errors and imperfections in the respective neuromorphic hardware devices [143], [144].

Despite that progress from the algorithm side, the (required) nonlinear behaviour of existing neuromorphic hardware implementations do not allow for a converging backpropagation. Thus, along with new hardware implementations such as k-NET, new algorithms need to be found to circumvent this issue such that SNNs outperform the ANNs of today in all means. Typical low-level realizations of SNNs exhibit a limited capacity for complex operations and training deep SNNs is a challenging task which has not succeeded to date.

Consequently, applying k-NET in form of a classical forward DNN with backpropagation and supervised learning is the most straightforward approach to start the integration of k-NETs disruptive approach into the neural networks of the future. In order to have a comparison for classification with the alternative technologies, we give a short, exemplary overview on classification tasks perform with other platforms for neuromorphic computing. For more information, we refer the interested reader to the references and references therein.

7.2. Classification tasks accomplished with different hardware approaches:

7.2.1. CMOS

Neuromorphic systems employing CMOS technology can be implemented in a fully digital or mixed digital-analogue manner. Specifically, the core-to-core interconnects utilize digital CMOS logic where the neurosynaptic core can also be analogue or mixed. Digital neurons can be realized by CMOS logic circuits as well whereas the analogue parts follow either a design based on sub-threshold current-mode or above-threshold circuits [57]. These systems utilized different learning platforms to perform the classification of handwritten digits, for instance [45]. As the oldest technology numerous

classification tasks have been performed with CMOS based technology and based on Si-CMOS technology several large-scale architectures which integrate more than 1000 neuron were built. Correspondingly these machines were utilized to perform various types of classification tasks or generally different types of learning algorithms were tested mostly with CMOS or with CMOS/Hybrid CMOS/memristive platforms. (cf. Table I). Other machines on large-scales are Dynap-Se or Odin ([44], [57], [145] and references therein) . Additionally, there are also small-scale approaches as well.

Table 1: *Overview on large and small scale mainly CMOS based architectures and their efficacy for specific classification takss including the utilized CMOS technology and energy consumption. The classification tasks are mainly handwritten digits or image recognition. More information can be found in the given references and references therein.*

Neuromorphic Chip	**Technology /Company**	**Neuron density**	**Synapses & Energy consumption**	**Classification tasks performed (exemplary, c.f. Refs as well)**
SpiNNaker[146]	Digital, 130 nm CMOS, efficient simulation large spiking networks (University of Manchester)	10^9 spiking neurons approaching brain complexity	100 nJ/neuron & 43 nJ/synapse	Spinnaker 2 prototype, DNN: Handwritten digits dataset MINST : 96.6 %[147] Audio sample classification : 85 % [148]
TrueNorth[30]	Digital CMOS, 28 nm process technology IBM	4096 neurosynaptic cores (10^6 neurons) [44], [57], [145] Leaky integrate and fire in each core	256 M synapses, 26 pJ/synaptic operation	Real-time classification EEG data [149] Handwritten digits & Protein secondary structure recognition [150]
Loihi[151]	Digital, 14 nm (FinFet) process CMOS, Intel	$130 \cdot 10^3$ neurons	$130 \cdot 10^6$ synapses 81 pJ/neuron & 15 pJ/synaptic operation	Gesture recognition, 89.64 % classification accuracy [152]
Neurogrid[153]/Braindrop[154]	Mixed signal 28 nm CMOS	Up to 10^6 neurons/4096 neurons, 64KB weight memory	0.38 pJ/synaptic update	

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BrainScaleS[155]	Mixed digital analogue. 180 nm (65 nm) CMOS first (second) generation	$180 \cdot 10^3$ neurons	$40 \cdot 10^6$ synapses per wafer 10 pJ per transmit	[156]Deep spiking neural network
Analog VMM	180 nm NOR flash		6-bit Analog Synapse resolution 20 nJ/inference	MNIST: 94.7 % Image recognition CIFAR-10: 84.8 %
Other small-scale algorithms cf. [23] **and references therein)**				
Supervised DNN [157]	ResNet: Backpropagation with ReLU			CIFAR-10 95.08 %
Supervised SNN with transfer learning LeNet network[24]	ConvNet Neuron with rate-based leaky integrate and fire neuron			MNIST handwritten digits recognition 99.44 %
Spike based backpropagation[158]	Backprop with rate based integrate and fire neurons			MNIST, accuracy 99.31%

For instance, a network based on two SST re-routed NOR-arrays realized in a three-layer ANN showed 94.7 % of classification fidelity within 1 µs and power consumption of 20 nJ per synaptic event but on the cost of increased cell-sizes due to the re-routing approach [56]. For more detailed information the reader may refer , for instance, to Ref. [23] and reference therein.

7.2.2. SPINTRONICS

Spintronic memristors

Spintronic memristors have a strong potential for linear classification and associative memory operations since the non-volatile memory, i.e., memristive devices, need to provide almost infinite endurance and almost instantaneous response capabilities. These criteria are met by spintronic devices.

For instance, memorization and pattern association could be demonstrated by using Hebbian learning on three kinds of 3x3 block patterns which converged after 20 iterations. In this work, spintronic artificial synapsed were combined with conventional electronics, where the first were comprised of SOT switching devices consisting of antiferromagnetic-ferromagnetic bilayers [159]. However, this field is in its infancy as well and still on the proof-of-concept level.

Synchronized spin-torque nano oscillators.

Using the spintronic based approach and reservoir computing methods, Romera et al. successfully demonstrated the classification of seven spoken vowels by a small network of four-coupled spintronic nano-oscillators. The training required less than 100 iterations with an accuracy of 84 % after cross-validation, exceeding the performance of executing the same task with a multilayer perceptron network.

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Although compact and low-power consuming, the oscillators in this approach need to be highly tuneable in frequency. The first results are promising but large-scale demonstration is yet to be realized. However, one disadvantage of magnetic tunnel junctions are small fluctuations in the resistance which complicated the read-out [26].

Superparamagnetic MTJs

The stochastic temperature dependent state fluctuations of superparamagnetic MTJs resemble Poisson spiking dynamics and can be used to emulate neural population coding.

Accordingly, that population coding and cascaded nonlinear operations with superparamagnetic MTJs were recently shown. That would, for instance, enable one to teach robots how to perform basic reactive movements such as grasping balls [160] while consuming substantial lower amounts of energy. That is 23 nJ (7.4 nJ) per operation during (after) learning compared to 330 nJ on CMOS based neurons.

Domain Wall and Skyrmion based neurons.

To date, there are only theoretical considerations and simulations that demonstrate that magnetic textures such as skyrmions can be used for reservoir computing and pattern classification, respectively [92], [93]. Similarly it accounts for DWs which could be used as domain wall oscillators- analogous to spin torque oscillator neural networks or for secure hardware classification tasks [161]–[164].

7.2.3. LOW-DIMENSIONAL STRUCTURES

As said, although promising, the current research of low-dimensional materials needs to yet be further explored on a fundamental research level and benchmarking, compact models and intense computational research are needed for nanoscale devices and future classification tasks. Notably, most current approaches are at still at the hardware level implementation [20].

7.2.4. Classification performed with memristor devices

Although impressive results with respect to image classification [165], face verification [166] and speech recognition [16], [161], [167] were achieved using von-Neumann architectures, the latency and high power consumption are problematic. Since memristive devices inherently supply in-memory computing, are highly energy efficient and fast using Ohm's or Kirchhoff's law, they are emerging as an alternative, where RRAM and PCM are particularly advanced. In parallel, as the latter are also limited for up-scaling such as non-linearity (**cf. section on memristive devices)**, new concepts with three terminal memristive devices such as ECRAM [168] or ionic floating gates [169] have been developed which partly overcome the aforementioned problems (**c.f. Figure 5** as well).

Crossbar architectures using DNNs were used for pattern classification both with RRAM and PCM based memristor units [35], [36], [169]–[172]. For instance, a crossbar array of 165000 PCM devices with a 1T1R (one transistor-one resistor) structure and implementing a three-layer DNN demonstrated image classification [35]. After the training using the MNIST database, the network achieved image classification with an accuracy of 83% due to the mentioned drawbacks of PCMS, that is asymmetry or nonlinearity of the PCM response [170]. An alteration of the synapse allowed to increase the accuracy of MINST classification to 92% [171] and grey-scale face classification from the Yale database with 91.5% accuracy. Using a 4kbit HfO_2 RRAM array with a novel programming scheme led to a maximal classification accuracy of 83% but simulations show accuracies >90% are possible.

SNNs encode the information in spikes, where a spike can represent the input signal by a real-valued signal (rate-encoding) or via the spike's latency (temporal coding) [23], [29]. The correlations between pre- and post-spike neuronal events are used to update the synaptic weights using a plasticity rule based on ''Hebbian Learning" which can be modulated by error feedback. The synaptic weight

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decreases in long-term depression (LTD) and increases for long-term-potentiation. The currently leading plasticity rule for SNNs, STDP, is a based on the time difference between the post-and prespikes [173]–[176].

Currently many SNNs are not able to perform on-chip learning but need to be pretrained off-chip first. This is due to the necessity of simultaneous access of all synaptic weights which increases critically the circuit overhead and hence the chip size. Despite this difficulty, both unsupervised STDP [177]–[179] and supervised STDP learning have been reported [180]–[182]. Possible applications such as data clustering or anomaly detection were discussed for an SNN, where the synaptic weights are updated by unsupervised STDP. The training of an ANN with a stochastic STDP was also shown, applied for the example of a visual pattern extraction utilizing RRAM based synapses. Additionally, by employing ferroelectric RAM (three terminal ferroelectric memristor), STDP supervised learning could be demonstrated [183]. A detailed comparison of off-chip unsupervised STDP and backpropagation for different memristor types and learning algorithms proves that STDP is by orders of magnitude more energy efficient than neural networks, as ~ nJ for the first and ~µJ for the latter [184] (and references therein). A memristor perceptron was trained to classify a stylized letter pattern with a memristor-based neuromorphic chip using different approaches such as ex situ or in- situ training [185], [186].

Limited reliability such as fatigue in ferroelectric RAM [186] or necessity of current control during set transition to avoid an uncontrolled growth of the conductive filament in RRAM [187] or sneak paths limiting the operation in crossbar arrays [188] render pure memristive devices for neuromorphic computing currently limited.

7.2.5. Hybrid CMOS-memristor devices for classification tasks

Alternatively, to overcome above limitations and realize large-scale neuromorphic circuits, hybrid CMOS- memristor devices are a promising route where the memristive devices is integrated into the end of a CMOS process (cf. Ref. [23] and references therein). For instance, using SNN with RRAM-CMOS synapses the pre-neuron can drive a large synaptic fanout using digital CMOS buffers and voltage waveform engineering is used to transfer the latency between pre- and post-spikes [23], [51], [189]. The former can then be applied in transfer learning for inference applications. Among others, current hybrid architectures are op-amp based neuron designs [190], [191] or even driven leaky integrate and fire neurons in 180nm CMOS technology which drove RRAM cross point arrays with in-situ STDP learning [192], [193].

Transfer learning, i.e., DNN to SNN conversion, allows one to initialize SNNs and use pretrained models at the input. The highest obtained accuracy with transfer learning is 99.44 % for a MNIST handwritten digits dataset [24], while DNN yields 99.79% classification accuracy[23], [194]. Detailed tables with training accuracy of hybrid CMOS-memristor approaches can be found in Ref. [23] and references therein. To overcome the accuracy gap between semi-supervised SNNs and DNNs using backpropagation, recently also spike based propagation training methods are also under intensive investigation [195]. However, as backpropagation emerged from classical von-Neumann architectures the old issue of latency and high-power consumption are back on stage. Thus, backpropagation suffers from weight-transport problems as the transpose of the weight matrix between the lth and the l+1 level must be available, nonconcurrence, high required precision of the derivatives in the backpropagation computation and the problem of assigning the temporal credit. OxRAM with 130 nm realized in a 2Kb differential RRAM are an example for a large-scale integration and on-chip inference employed for different datasets [196]. A similar RRAM ut using an FPGA back-end demonstrated a MNIST accuracy of 94.4 % [197] and TaOx/HfO2 RRAMs with 130 nm CMOS showed 96.5 % accuracy [198].

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7.2.6. Classification tasks with Photonics

Although comparably complex, photonic reservoir-based computing approaches have been used for first demonstrations of classification tasks. For instance, spoken digits could be classified with a single optoelectronic modulator and an optical fibre and a reservoir computer based on light-modulators was employed to perform the recognition of human action by computer vision [199], [200].

By using a photonic neural network, tasks such as audio or image classification, nonlinear optimization or neuroscientific hypothesis testing have been already demonstrated with recurrent, feed-forward and spiking and feed-forward neural networks respectively[60], [65], [108], [201].

Compared to other approaches for neuromorphic computing the interconnectivity and linear operations of photonic based networks are their biggest asset. However, the interconnectivity is still achieved in real space opposite to k-NET and photonic based neuromorphic computing is facing several challenges to date. One promising approach uses scalable silicon based photonic platforms, but these platforms do not currently can generate light on-chip. This renders the required co-packaging of electronics and light-sources critical for the efficiency, scalability, and stability and in the end energy consumption of the photonic neural networks. Furthermore, resonance trimming to counteract environmental variability in integrated photonics due to the built-in resonant devices is necessary and enhance the systems complexity (Ref. [25] and references therein) . Additionally, building blocks such as logic gates or memory are still lacking for (pure) photonic platforms, which is realizable with magnonics and k-NET on the contrary.

8. Conclusion on report for deliverable 4.1 and classification directives for k-NET

In summary, we have given an overview of the state-of the art on alternative (mostly hardware-based) platforms for neuromorphic computing and artificial intelligence for the industry 4.0. Furthermore, it contains an overview on the performed classification tasks with the different alternative technologies and a discussion on the general advantages of magnonic based approaches and in particular k-NET. Although the technologically most advanced approaches for neural networks based on CMOS and CMOS-memristor hybrid platforms demonstrated classification accuracies >99% for specific tasks such as handwritten digits recognition, the circuitry remains complex and still required substantial energy amounts.

As stated in the beginning, this report represents the Deliverable 4.1 of work package for under the lead of Thales at month 12 of the k-NET project.

As stated earlier, due to the unique operation in wavevector space,k-NET inherently does not require wiring between neurons and synapses. The neurons and synapses in k-NET correspond to the spin wave mode amplitudes (populations) and to the nonlinear interactions among them, respectively. These nonlinear interactions will result in a time dependent evolution of k-NET neurons. Hence, contrary to a feedforward (deep) neural network there is no clear one-way propagation path and then the system will be inherently recurrent as well. For example, a given input mode population may not only be affected by the input signals, but also subsequent spin-wave scattering processes. As a result, energy therefore flows in and out of these modes in a complex way, until a readout is made. Consequently, that inherent properties of k-NET will impose some bounds on the training techniques that one could use.

Being only one type of imaginable neural network, k-NET could be classified as a Hopfield-like device.

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Hopfield type neural networks are recurrent ANNs which are typically used for auto-association and optimization tasks.

Additionally, note that- at this stage- we anticipate that the k-NET concept will be useful for classifying tasks for which information is naturally encoded in frequency space. For example, we can envisage greatly extending the vowel recognition task of Romera *et al.*, where formants, i.e., resonant frequencies of the vocal tract that characterize a particular vowel, are used as inputs to a spin-torque nano-oscillator array. In the k-NET device, these frequency inputs can be mapped onto specific spin wave mode populations, whose nonlinear interactions would lead to distinct output states of the magnetic system. Because the ferromagnetic element used possesses a greater number of accessible states (N >> 4) in comparison to an oscillator array, we anticipate that classification schemes can be applied to datasets with large number of members.

We must emphasize that vowel recognition is an excellent and widely used toy problem to test neuromorphic computing models with emerging devices. Furthermore, employing vowel recognition as a test problem, allows a straightforward approach to benchmark our results against literature work. While a central goal of the project is demonstrate such a toy problem, we expect that k-NET devices will be scalable to larger sizes and / or interconnected to form complex processing pipelines. These, eventually, should excel in complex recognition tasks. For instance, one utility of the spin wave neural network is the capacity to process GHz-rate signals “natively” without too much pre-processing. In this light, one could also think about applications such as feature detection in radar data (e.g., autonomous vehicles).

However, one must also not that there are numerous nonlinear spin wave processes that involve clear thresholds which might mimic integrate-and- fire behaviour. Thus, at this stage of the project a possible realization of the K-NET conjuncture as a SNN has to be considered, either. The involvement of thresholds determines a specific energy regime for onset the nonlinear spin wave interactions, i.e., scattering processes. If the system is driven in a clocked manner, the (multiple) spin wave scattering processes result in an energy redistribution of the spin wave modes, that is k-NETs neurons such that the system falls again below the critical threshold and needs to be ‘pumped’ above with the next incoming signal. Such functionality would exhibit some analogies with leaky integrate and fire behaviour of SNNs.

In combination with the given overview on the state-of the art of alternative technologies of k-NET and their classification tasks and the previous discussion shows what are the current limitations of the other technologies and that K-NET has the potential to be possibly used in different types of neural networks which widens the area of application of k-NET wavevector spaced approach. Hence, it could be indeed a game changer which needs to be further classified in the future and will be part of the deliverable D 4.2 at month 18.

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